High-Performance CPU-Prototype System Testbed Design, Construction and Evaluation

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1 Background

Higher and higher performance requirements for uni-processing are never-ending. Some years ago a temperature-wall was reached in uniprocessor design ending the possibility of future increases in clock frequency to improve performance. In the internal architecture (or microarchitecture) dimension of performance, existing structures and methods of executing more instructions in a cycle reached a point of ever-diminishing returns: current cores only execute one-to-two instructions-per-cycle.

Industry's response to these situations was to put more than one uniprocessor (or core) on a chip. These multicore processors are only able to realize significantly better performance via difficult parallel-programming or re-programming; sometimes even these do not work.

2 Project Details: *Teradactyl Prototype System*

Teradactyl is a high-performance uniprocessor prototype targeted to execute 10 (ten) or more instructions-per-cycle automatically, without any parallel-programming effort by a user. The goal of this project is to complete the design, construction, testing and experimental evaluation of the Teradactyl system. This is a research project, and we expect to publish the results.

In order to fully test and evaluate Teradactyl it is necessary to create a testbed system. The latter will consist of many COTS (Commercial Off-The-Shelf) FPGA boards, interconnected via custom boards and standard cables. The latter boards are to contain a PC-controlled variable power supply, temperature and voltage sensor circuitry and associated A/D and D/A elements. The custom boards will be identical. All of the FPGAs will contain the same logic.

This project requires both a computer engineer and an electrical engineer having skills in some or all of the following areas (note: at least one engineer must be proficient at VHDL design):

1. System architecture, e.g., host PC to Teradactyl interface and control
2. Microarchitecture (sub-system design), e.g., Teradactyl memory system design
3. Software and firmware design, e.g., PC host program, FPGA internal control
4. VHDL logic design, i.e., for all of the logic held in the FPGA
5. Analog sensor and control circuitry, for temperature and power measurements
6. Variable power supply design and control with op-amps

3 Deliverables

- ◊ Detailed documentation of the hardware and software designs
- ◊ Results of Teradactyl measurements and evaluation